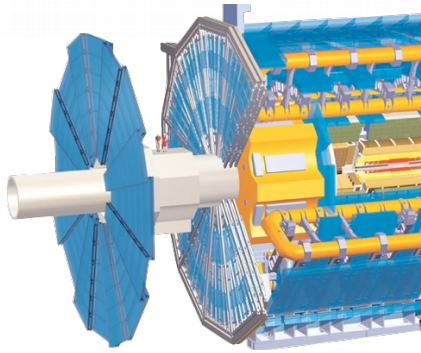
TEXAS
The University of Texas at Austin

ATLAS EXPERIMENT



Integration Plan Summary (so far)

Ray Xu

Mar 24, 2017

Outline

- Last Consensus of Project SAR + DRE (production chip)
  - Input Selection
  - Power sharing
  - Clock sharing
  - Packaging & real-estate
  - I/O's & Scan chain
- Quick update on SEU readout

Last Consensus

- Two Chips on one real-estate
- Production Chip (*Pad-limited*) (**the focus of next slides**)
  - Project SAR
  - DRE
  - SEU Detector
  - Scan chain + input selection between DRE/SAR
  - Padframe prepared by Jaro
- Experimental SAR Chip (*Autonomy*)
  - No IP-cell pads
- Jaro has new proposition?

Input Selection

- On production chip: only one DRE and one project SAR
- Desire to bypass either block
- DRE
  - Two (three?) outputs
  - One goes to project SAR
  - Others go off-chip
- Project SAR
  - Two inputs
  - Enable/disable clock to one of two input bootstrap SW
  - One is off-chip input, other goes to DRE output

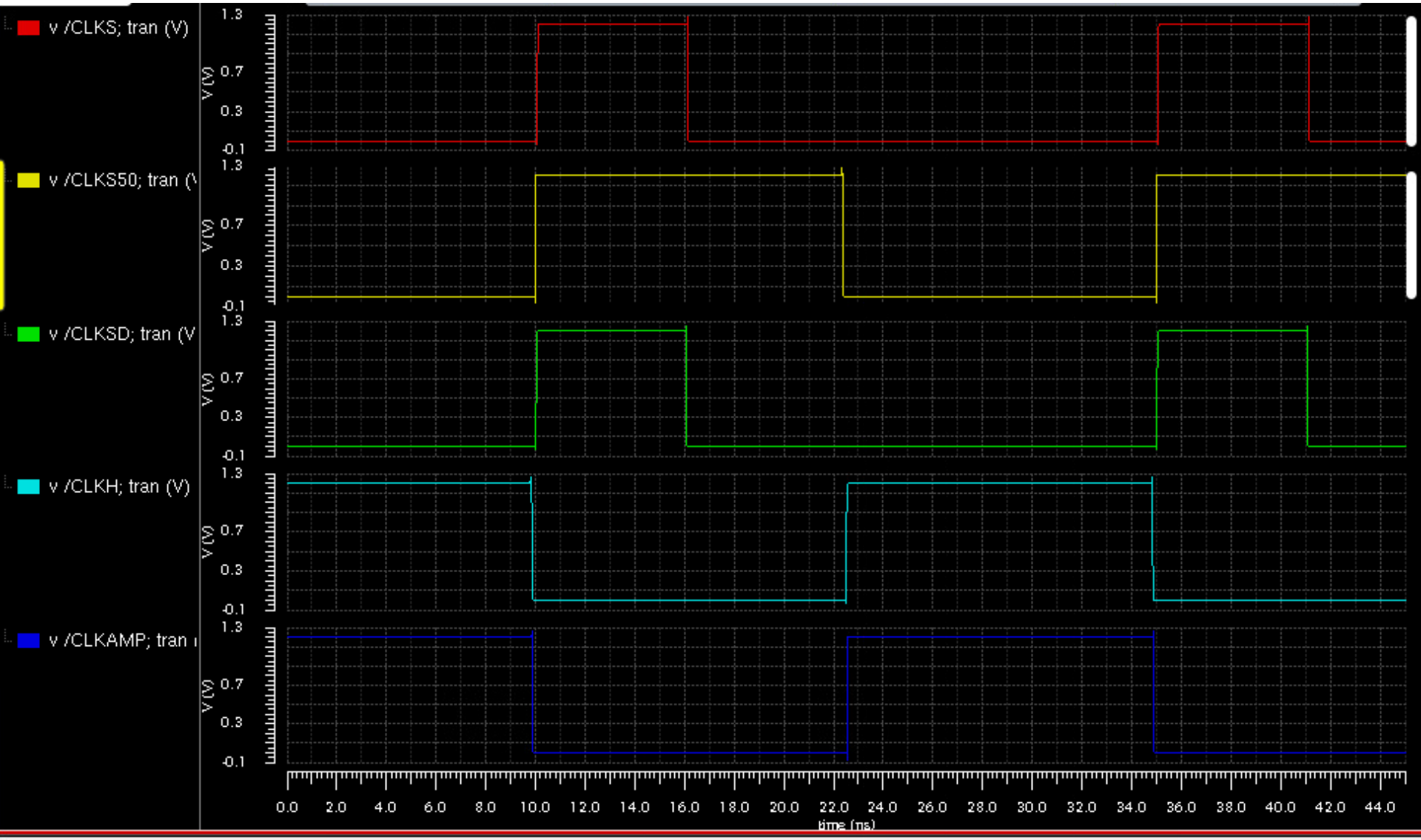
Power Sharing

- +1.2V DVDD and AVDD shared amongst SAR, DRE, and SEU
- +2.5V AVDD?
- Power both the SAR+DRE+SEU simultaneously
- Disable either block via clock gating or under-biasing
- Do we need more power regions?

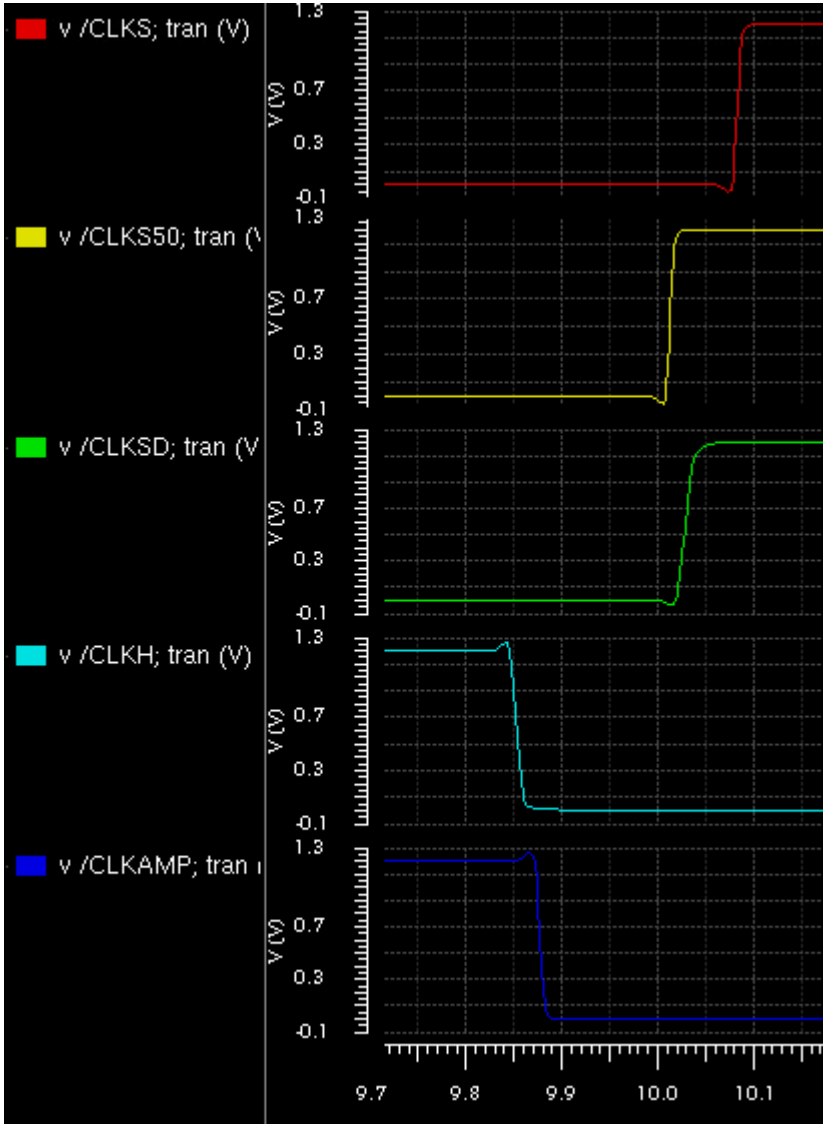
Clock Sharing

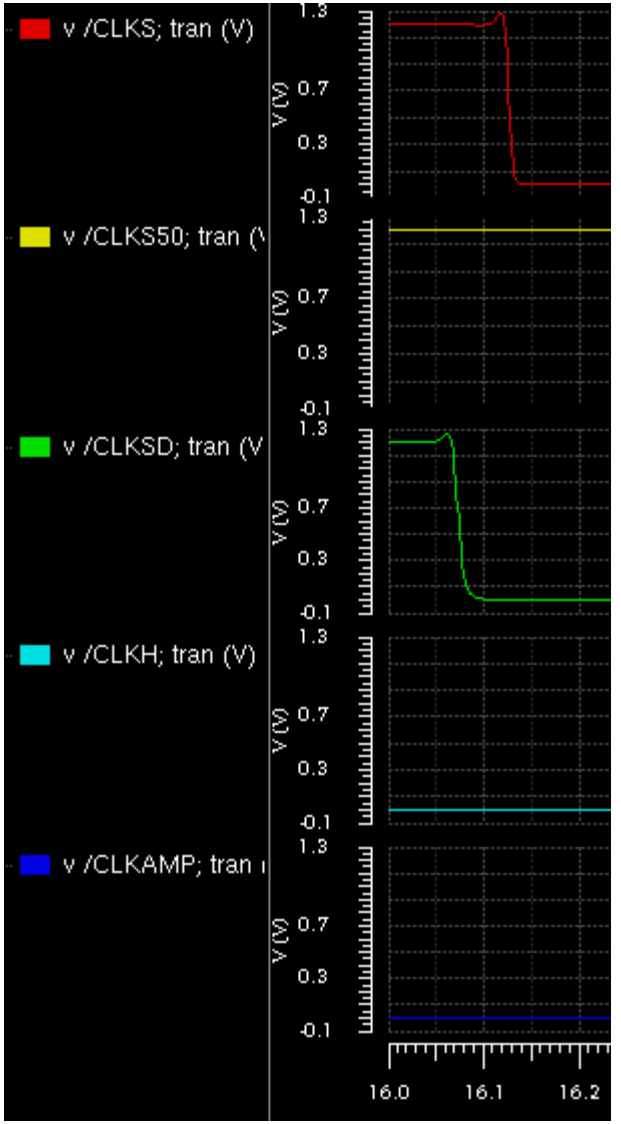
- (Mostly for Sarthak)
- See cell “rxu_ckhClkDiv_testbench”
- Sampling clock (ClkS and ClkSD) goes high → 1pF load is presented @ SAR input
- 160MHz external input → 40MHz phases
- Next few waveforms shown with no load capacitance

Clock Sharing



Clock Sharing





Packaging & Real-Estate

- Target silicon: approx 2mm x 2mm, 72 pins minus GND
- 1p6m 3X1Z1U
- Package carrier
  - 10mm x 10mm
  - Exposed ground pad
  - 4mm bondwire
- Package+bondwire parasitics: 0.9pF, 4nH, 4 Ohms
- Socket parasitics: <0.3pF, 0.6nH

I/O's and Scan-Chain

- Listed below are tentative
- Project SAR + SEU Detector:
  - Minimum 40 analog/digital I/O's for SAR+SEU
  - Minimum 4 control bits for SEU Detector scan-chain
  - SAR scan-chain TBD
- DRE:
  - Minimum 34 analog/digital I/O's
  - Minimum 17 control bits
- Experimental ADC:
  - 20-30 total pads?
  - Scan chain?

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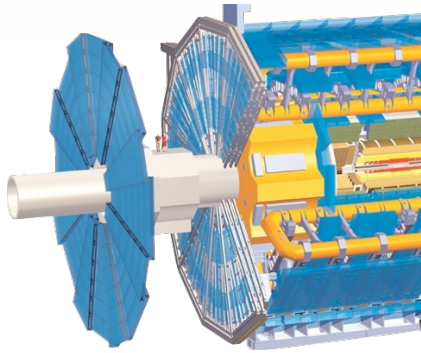

Update on SEU Detector Readout

SAR SEU Readout

- 4 out of 32 coarse DAC unit caps are monitored
  - 4 electrometer OTA's
  - 4 simultaneous analog outputs
- Additional test-structure detectors, some using dummy DAC caps.
  - Independent of SAR ADC operation
  - Readout circuitry need not to be as fast/high-performance.

Electrometer OTA

- Single-ended 2-stage with buffer
  - DC Offset: observe DC output before irradiation (for now). Keep gain low.
  - Noise: 800uV input referred noise
  - Gain w/ R feedback: 3x (9dB) (may be increased)
  - Open-loop gain: 30dB
  - Input cap: 1fF
  - f-3dB = 200MHz (rise/fall time = 1.8nS), 85 deg. PM, w/ 20pF load
  - 700uW per OTA